Abstract

An area-effective 12-bit linear digital-to-analog converter (DAC) of source driver is proposed for large-size TFT-LCDs. The proposed DAC is composed of resistor-string DAC for MSB 6-bit, current DAC for LSB 6-bit and interpolation amplifiers. To reduce the area of DAC, 6-bit current DAC is designed using low voltage devices. We designed and fabricated the source driver with the proposed DAC using 0.13 μm process with 2.5 V low voltage devices and 16 V high voltage devices. One channel layout area is 17.5 μm × 600 μm, which is shrunk by 15% compared with that of 8-bit resistor-string DAC. The experimental results show that the output voltage deviation is less than 3.5 mV.

1. Introduction

Liquid crystal display (LCD) is a typical flat panel display widely used as the display unit of the cellular phones, laptops, monitors of desktop computers, and televisions. The demand for image-quality improvement of the LCD has increased rapidly, from 8-bit to 12-bit color depth, from full high-definition (HD) resolution (1920×1080) for digital broadcasting to QUXGA (3840×2400) for digital cinema and from 40-inch to 100-inch for large-size displays [1-2]. Thus, the gray scale of digital-to-analog converter (DAC) in source driver ICs for LCD should increase.

DACs in source driver ICs for LCD systems play a role of generating analog output voltages for driving liquid crystal from digital input data. Moreover, each channel in source driver ICs needs at least one DAC. Thus, total area of DACs in source driver ICs is large because source driver ICs has hundreds of channels. Therefore, DACs require uniform performances in data channels and compactness in chip occupation area as well as low power consumption. The resistor-string DAC (R-DAC) architecture has been mainly used owing to its uniform characteristics, because each R-DAC in data channels shares a common resistor-string for reference voltage generation. Meanwhile, the increase in color depth for AMLCDs discloses the limitation of the R-DAC architecture. For an 8-bit AMLCD source driver IC, the R-DAC requires large area for its decoder and related routing lines connecting several hundreds of channels to the common resistor-string, and the occupation area exceeds more than 60% of the overall driver IC [2]. Besides, the area of R-DAC doubles for the 1-bit increase in the image data. Therefore, the required area will increase four times in case of 10 bit AMLCD source drivers for TV applications so that the source driver with 10-bit R-DAC is impractical.

Many researchers have attempted to reduce the DAC’s area with high gray scale, such as resistor-resistor-string DAC [2], charge re-distributed DAC [3], embedded DAC using LSB interpolation [4], and segmented resistor-capacitor DAC [1]. The resistor-resistor-string DAC needs sub resistor-string DAC with high resistance so that increase of DAC’s area and long digital-to-analog (DA) conversion time can occur. The charge re-distributed DAC suffers from long digital-to-analog conversion time due to serial 1-bit by 1-bit DA conversion. Thus, there need two DACs and buffers in a channel to overcome long conversion time so that it is not adequate to apply to high-resolution and large-size TFT-LCDs. The embedded DAC using LSB interpolation requires a large number of input-pair transistors in an amplifier. Moreover, the transistors require large width and length for accurate matching characteristics, leading to the area penalty of the amplifier for high bit interpolation. The segmented resistor-capacitor DACs are susceptible to the process variation, charge injection error, and the clock feedthrough error of switches. Moreover, there are two sample-and-hold buffers each channel because the time to charge the capacitors in a sample-and-hold buffer is long.

To solve these problems, we proposed the area-effective hybrid type DAC with current-DAC and interpolation buffer amplifier. Especially to reduce the area of DAC, the current-DAC is designed using low voltage devices without additional high voltage circuits such as level shifter and buffer. Thus, the one channel layout area could be shrunk by 15% compared with that of 8-bit R-DAC.

2. Proposed 12-bit linear DAC

Figure 1 shows the block diagram of two channels in source driver with resistor-string DAC for MSB 6-bit and current DAC.
for LSB 6-bit and interpolation amplifier. In addition, for high-quality image, we adapted dot inversion method for polarity reversal. The amplifier PAMP with the push function operates in a positive gamma range and the amplifier NAMP with the pull function operates in a negative gamma range, respectively. We sequentially connected each channel to either the amplifier PAMP or the amplifier NAMP by controlling the polarity control signal.

Figure 2 shows a schematic of the 6-bit current-DAC with an interpolating buffer amp. The negative feedback loop is composed of the amplifier AMP1 and the transistor N1, and the voltage drop across the resistor \( R_1 \) is the same value as the \( V_{REF} \), which is the positive input voltage of the amp AMP1. And then, the current \( I_{REF} \), which is proportional to the \( V_{REF} \), is generated through the \( R_1 \), and the 6-bit current DAC selects one of binary weighted 64 currents. In the case of the NAMP, the selected current is directly pulled from the resistor \( R_2 \). On the other hand, in the case of the PAMP, the selected current is pushed to the resistor \( R_2 \) through a cascode current mirror. Therefore, the output voltage for positive gamma and negative gamma can be expressed as equation (1) and (2), respectively

\[
V_{OUT} = V_{COARSE} + \frac{R_2}{R_1} \cdot V_{REF} \cdot \frac{1}{2^n} \sum_{n=0}^{\infty} O < n > \cdot 2^n \\
V_{OUT} = V_{COARSE} - \frac{R_2}{R_1} \cdot V_{REF} \cdot \frac{1}{2^n} \sum_{n=0}^{\infty} E < n > \cdot 2^n
\]

where \( V_{OUT} \) is the output voltage of buffer amplifier, \( V_{COARSE} \) is the selected output voltage from MSB 6-bit resistor-string DAC, \( V_{REF} \) is the reference voltage for current generation circuits, \( O < n > \) is the LSB 6-bit data input code of odd channel and \( E < n > \) is the LSB 6-bit data input code of even channel, respectively.

The minimum output voltage gap from MSB 6-bit R-DAC is less than 150 mV, which is the maximum voltage interpolated by LSB 6-bit current DAC so that we designed 6-bit current DAC using the low-voltage devices as shown in Figure 2. It leads to reduce the DAC layout area because low voltage devices have superior matching characteristics to high voltage devices so that small size transistors are available. Moreover, it can be removed additional circuits such as level shifter and inverter using high voltage devices. To connect this low voltage current DAC output and high voltage buffer amplifier, we inserted the protection transistor NH1. And then we optimized the transistor size and bias voltage so that the low voltage circuit cannot be destroyed by high voltage.

To obtain the accurate DAC outputs and good channel-to-channel output uniformity, we can use \( kR_2 \) instead of \( R_2 \), which means \( k \) times \( R_1 \) resistance values. Also, we can use the reference voltage, \( kV_{REF} \). In this case, the voltage drop across \( R_2 \) should be also divided by \( k \). We can control the ratio of \( R_1 \) and \( R_2 \) so that we can obtain the expected channel output. By using the \( kV_{REF} \) reference, we can reduce by a \( 1/k \) factor the offset of amplifier AMP1 that affect the 6-bit current-DAC output. Thus, it is possible to obtain good uniformity of the channel output. Moreover, to minimize the process mismatch errors of resistance, we used one common current reference circuit every six channels and located \( R_1 \) and \( R_2 \) closely and optimized the layout.

Figure 3 show the simulation results of output characteristics in source driver with the proposed DAC. As shown in figure 3, DNL and INL are less than 0.4 LSB, which 1 LSB is 1.8 mV. We can prevent breaking the monotony every 64 grays by optimizing the amplifier AMP1 and the reference voltage, \( V_{REF} \).
3. Measurement Results
We fabricated eighteen channels with the proposed 12-bit linear DAC using 0.13 μm process with 2.5 V low voltage devices and 16 V high voltage devices. Figure 4(a) and 4(b) show layouts of six channels of source driver IC with conventional 8-bit R-DAC and the proposed 12-bit linear DAC, respectively. One channel layout area adopted the proposed DAC 17.5 μm × 600 μm, which is shrunk by 15% compared with that of 8-bit R-DAC. Figure 5 shows the measured output characteristics of eighteen channels in source driver. As shown in Figure 5(a), the measured output voltage is linear and monotonous. The channel-to-channel mismatching due to the offset of AMP1 and mismatching of resistors is solved by optimizing the AMP1 and resistor layout. The measured output voltage deviation is less than 3.5mV as shown Figure 5(b) and 5(c). The feature of the proposed 12-bit linear DAC is summarized in Table 1.

4. Conclusions
An area-effective 12-bit linear DAC in source driver is proposed for large-size LCDs. The proposed DAC is composed of resistor-string DAC for MSB 6-bit, current DAC for LSB 6-bit, and interpolation amplifier. To reduce the area of DAC, 6-bit current DAC is designed using low voltage devices. The ratio between two resistors and the layout optimization is performed to obtain the accurate output characteristics. The simulation results show that both INL and DNL are less than 0.4 LSB. Its one channel
layout area is 17.5 μm × 600 μm, which is shrunk by 15% compared with conventional 8-bit resistor-string DAC with 0.13 μm process with 2.5 V low voltage devices and 16 V high voltage devices. The experimental results show that the output voltage deviation is less than 3.5 mV. Therefore, the proposed DAC is effective solution to make low-cost source driver ICs for high-resolution and large-size LCDs.

5. References


Table 1. Performance summary

<table>
<thead>
<tr>
<th>Process</th>
<th>0.13μm CMOS process with 16V high voltage devices</th>
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<tbody>
<tr>
<td>Number of gray scale</td>
<td>4096</td>
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<tr>
<td>Supply voltage for logic (Included current DAC)</td>
<td>2.5 V</td>
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<tr>
<td>Supply voltage for liquid crystal</td>
<td>15.5 V</td>
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<tr>
<td>Output voltage deviation</td>
<td>±3.5 mV</td>
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<tr>
<td>Power consumption</td>
<td>5 μA / channel for current DAC 10 μA / channel for output buffer</td>
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<tr>
<td>One channel layout area (From shift register to output)</td>
<td>17.5 μm × 600 μm</td>
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<td>(15% shrinkage compared with conventional 8-bit R-DAC)</td>
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